FP6805

Microprocessor Reset Circuits With Adjustable Delay Time

Description

The FP6805 asserts a reset signal whenever the V_{DD} supply voltage declines below the preset threshold and monitors the system voltages from 0.4V to 5V. A time delayed reset can be accomplished with an additional external capacitor. The FP6805 quiescent current is very low and suitable for portable and battery-operated applications.

The output $\overline{RST}$(RST) signal is set to be active low(high). $\overline{RST}$(RST) remains low(high) for the delay time after reset condition is deasserted and then goes high(low). The FP6805 provides ± 1% threshold accuracy.

FP6805 is available in space-saving TSOT-23-3, TSOT-23-5, TSOT-23-6 and TDFN-6 (2mmx2mm) packages.

Features

- Power-On Reset Generator with Adjustable Delay Time: 2ms to 10s (FP6805S9, FP6805D7)
  - C_d Pin Open: $\overline{RST}$(RST) Delay 240ms Typical
  - C_d Pin Connected to V_{DD} through a Resistor between 100kΩ: $\overline{RST}$(RST) Delay 0ms Typical
  - Capacitor Adjustable Delay Time
- Very Low Quiescent Current:
  1.5μA Typical (FP6805S9, FP6805D7)
  2.5μA Typical (FP6805S7, FP6805S8)
- High Threshold Accuracy: ± 1% Typical
- Fixed Threshold Voltages for Standard Voltage Rails from 0.8V to 5V (FP6805S9, FP6805D7), 1.5V to 5V (FP6805S7, FP6805S8) and Adjustable Voltage Down to 0.4V are Available (FP6805S9, FP6805D7)
- Manual Reset ($\overline{MR}$) Input
- Open-Drain $\overline{RST}$(RST) Output
- Immune to Short Negative SENSE Voltage
- Guarantee Reset Valid to V_{DD}=0.8V
- Available in TSOT-23-3, TSOT-23-5, TSOT-23-6 and TDFN-6 (2mmx2mm) Packages

Applications

- Notebook
- TV
- DVD
- Smart Phone
- STB

Ordering Information

FP6805-□□□

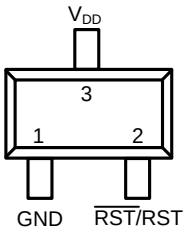
Package Type
S7: TSOT-23-3
S8: TSOT-23-5
S9: TSOT-23-6
D7: TDFN-6 (2mmx2mm)

RESET
A: Active Low
B: Active High

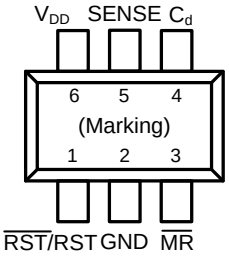
Threshold Voltage (V_{TH})
Blank: Adjustable
22: 2.2V 27: 2.7V 31: 3.1V
23: 2.3V 28: 2.8V 40: 4.0V
26: 2.6V 29: 2.9V 44: 4.4V
46: 4.6V

Pin Assignments

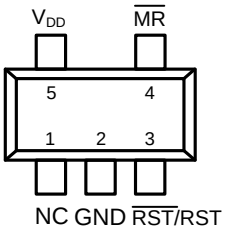
S7 Package: TSOT-23-3



S9 Package: TSOT-23-6



S8 Package: TSOT-23-5



D7 Package: TDFN-6 (2mmx2mm)

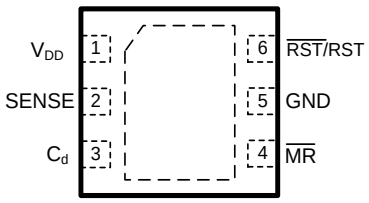


Figure 1. Pin Assignment of FP6805

TSOT-23-3 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805-22AS7	**Gk5**	2.2V
FP6805-23AS7	**Gk6**	2.3V
FP6805-26AS7	**Gi5**	2.6V
FP6805-27AS7	**Gk7**	2.7V
FP6805-28AS7	**Gk8**	2.8V
FP6805-29AS7	**Gi6**	2.9V
FP6805-31AS7	**Gk9**	3.1V
FP6805-40AS7	**Gm0**	4.0V
FP6805-44AS7	**Gm1**	4.4V
FP6805-46AS7	**Gm2**	4.6V

TSOT-23-6 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805AS9	**Gi9**	Adjustable
FP6805-22AS9	**Gm3**	2.2V
FP6805-23AS9	**Gm4**	2.3V
FP6805-26AS9	**Gm5**	2.6V
FP6805-27AS9	**Gm6**	2.7V
FP6805-28AS9	**Gm7**	2.8V
FP6805-29AS9	**Gm8**	2.9V
FP6805-31AS9	**Gm9**	3.1V
FP6805-40AS9	**Gn0**	4.0V
FP6805-44AS9	**Gn1**	4.4V
FP6805-46AS9	**Gn2**	4.6V

TSOT-23-5 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805-22AS8	**Gr3**	2.2V
FP6805-23AS8	**Gr4**	2.3V
FP6805-26AS8	**Gi7**	2.6V
FP6805-27AS8	**Gn5**	2.7V
FP6805-28AS8	**Gn6**	2.8V
FP6805-29AS8	**Gr8**	2.9V
FP6805-31AS8	**Gr9**	3.1V
FP6805-40AS8	**Gs0**	4.0V
FP6805-44AS8	**Gs1**	4.4V
FP6805-46AS8	**Gs2**	4.6V

TDFN-6 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805AD7	**Gr2**	Adjustable

TSOT-23-3 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805-22BS7	**GU1**	2.2V
FP6805-23BS7	**GU2**	2.3V
FP6805-26BS7	**GU3**	2.6V
FP6805-27BS7	**GU4**	2.7V
FP6805-28BS7	**GU5**	2.8V
FP6805-29BS7	**GU6**	2.9V
FP6805-31BS7	**GU7**	3.1V
FP6805-40BS7	**GU8**	4.0V
FP6805-44BS7	**GU9**	4.4V
FP6805-46BS7	**GV0**	4.6V

TSOT-23-6 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805BS9	**GS9**	Adjustable
FP6805-22BS9	**GV1**	2.2V
FP6805-23BS9	**GV2**	2.3V
FP6805-26BS9	**GV3**	2.6V
FP6805-27BS9	**GV4**	2.7V
FP6805-28BS9	**GV5**	2.8V
FP6805-29BS9	**GV6**	2.9V
FP6805-31BS9	**GV7**	3.1V
FP6805-40BS9	**GV8**	4.0V
FP6805-44BS9	**GV9**	4.4V
FP6805-46BS9	**GW0**	4.6V

TSOT-23-5 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805-22BS8	**Gn3**	2.2V
FP6805-23BS8	**Gn4**	2.3V
FP6805-26BS8	**Gr5**	2.6V
FP6805-27BS8	**Gr6**	2.7V
FP6805-28BS8	**Gr7**	2.8V
FP6805-29BS8	**Gi8**	2.9V
FP6805-31BS8	**Gn7**	3.1V
FP6805-40BS8	**Gn8**	4.0V
FP6805-44BS8	**Gn9**	4.4V
FP6805-46BS8	**Gr0**	4.6V

TDFN-6 Marking

Part Number	Product Code	Operation Supply Voltage
FP6805BD7	**GU0**	Adjustable

Typical Application Circuit

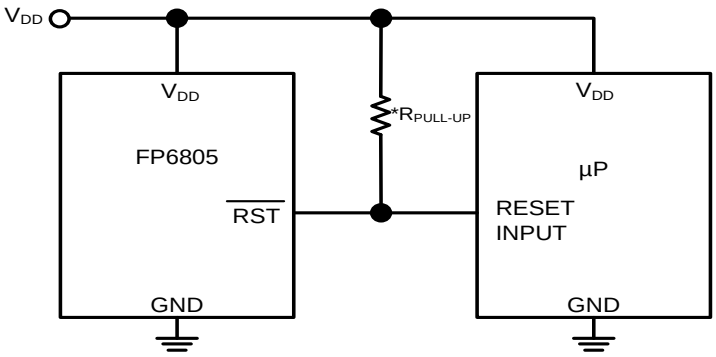


Figure 2. Typical Application Circuit of FP6805S7

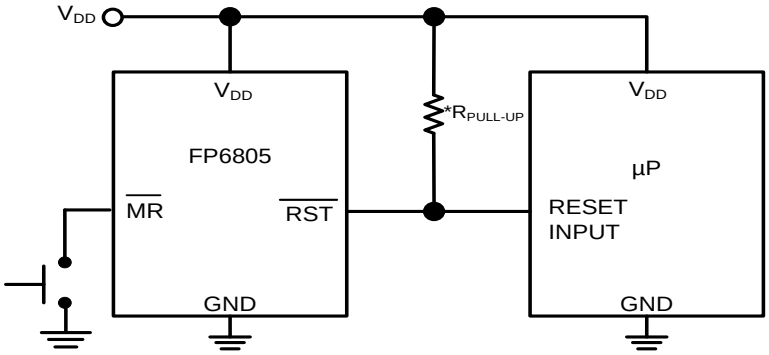


Figure 3. Typical Application Circuit of FP6805S8

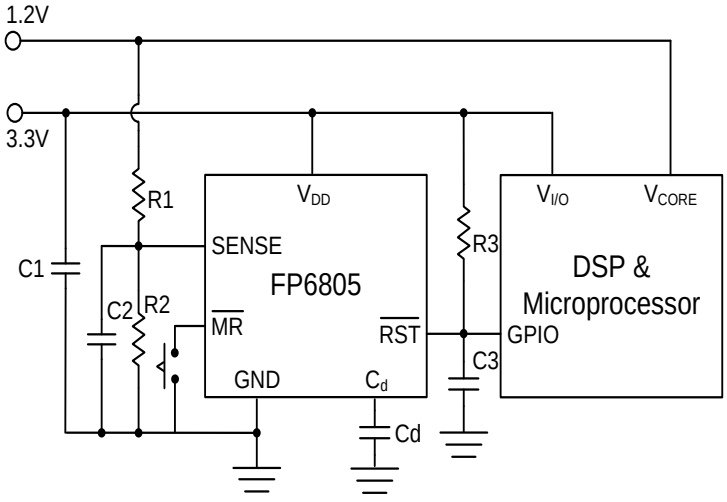


Figure 4. Typical Application Circuit of FP6805S9/FP6805D7

Functional Pin Description

Pin Name	Pin No. (TSOT-23-6)	Pin No. (TDFN-6)	Pin Function
$\overline{RST}$/RST	1	6	Open-drain reset output. $\overline{RST}$ remains low for the reset delay time after both SENSE is above V_{TH} and $\overline{MR}$ is set to a logic high. RST remains high for the reset delay time after both SENSE is above V_{TH} and $\overline{MR}$ is set to a logic high. A pull up resistor from 10kΩ to 1MΩ should be placed from this pin to V_{DD}.
GND	2	5	Ground.
$\overline{MR}$	3	4	Manual reset input. Pull $\overline{MR}$ low to manually reset the device. $\overline{MR}$ is internally tied to V_{DD} through a 110kΩ pull up resistor.
C_d	4	3	Reset delay time set pin. Connect a capacitor≧150pF between C_d and GND to set the delay time.
SENSE	5	2	This pin is connected to the voltage to be monitored. If the voltage at this pin drops below the threshold voltage V_{TH}, $\overline{RST}$ will be asserted.
V_{DD}	6	1	Supply voltage. V_{DD} is the power supply input, and it is recommended to add a 0.1μF ceramic capacitor close to this pin.

Pin Name	Pin No. (TSOT-23-5)	Pin No. (TSOT-23-3)	Pin Function
NC	1	--	Non-functional pins.
GND	2	1	Ground.
$\overline{RST}$/RST	3	2	Open-drain reset output. $\overline{RST}$ remains low for the reset delay time after both SENSE is above V_{TH} and $\overline{MR}$ is set to a logic high. RST remains high for the reset delay time after both SENSE is above V_{TH} and $\overline{MR}$ is set to a logic high. A pull up resistor from 10kΩ to 1MΩ should be placed from this pin to V_{DD}.
$\overline{MR}$	4	--	Manual reset input. Pull $\overline{MR}$ low to manually reset the device. $\overline{MR}$ is internally tied to V_{DD} through a 110kΩ pull up resistor.
V_{DD}	5	3	Supply voltage. V_{DD} is the power supply input, and it is recommended to add a 0.1μF ceramic capacitor close to this pin.

Block Diagram

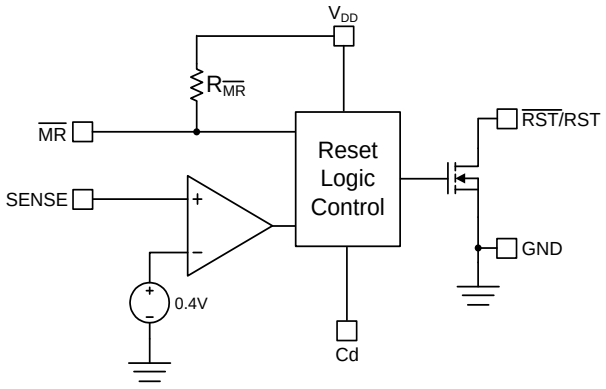


Figure 5. Adjustable Output of FP6805S9/FP6805D7

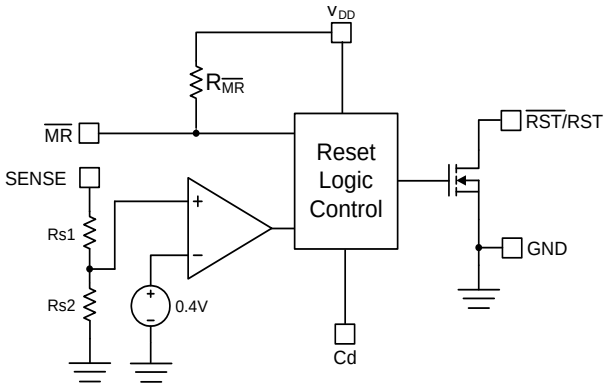


Figure 6. Fixed Output of FP6805S9

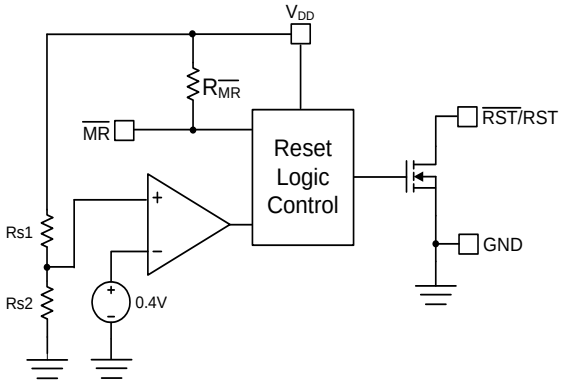


Figure 7. Fixed Output of FP6805S8

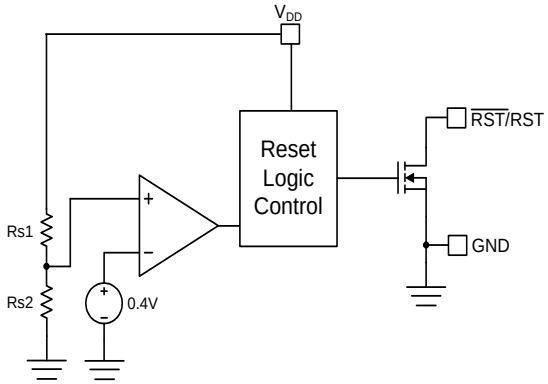


Figure 8. Fixed Output of FP6805S7

Power Timing Chart

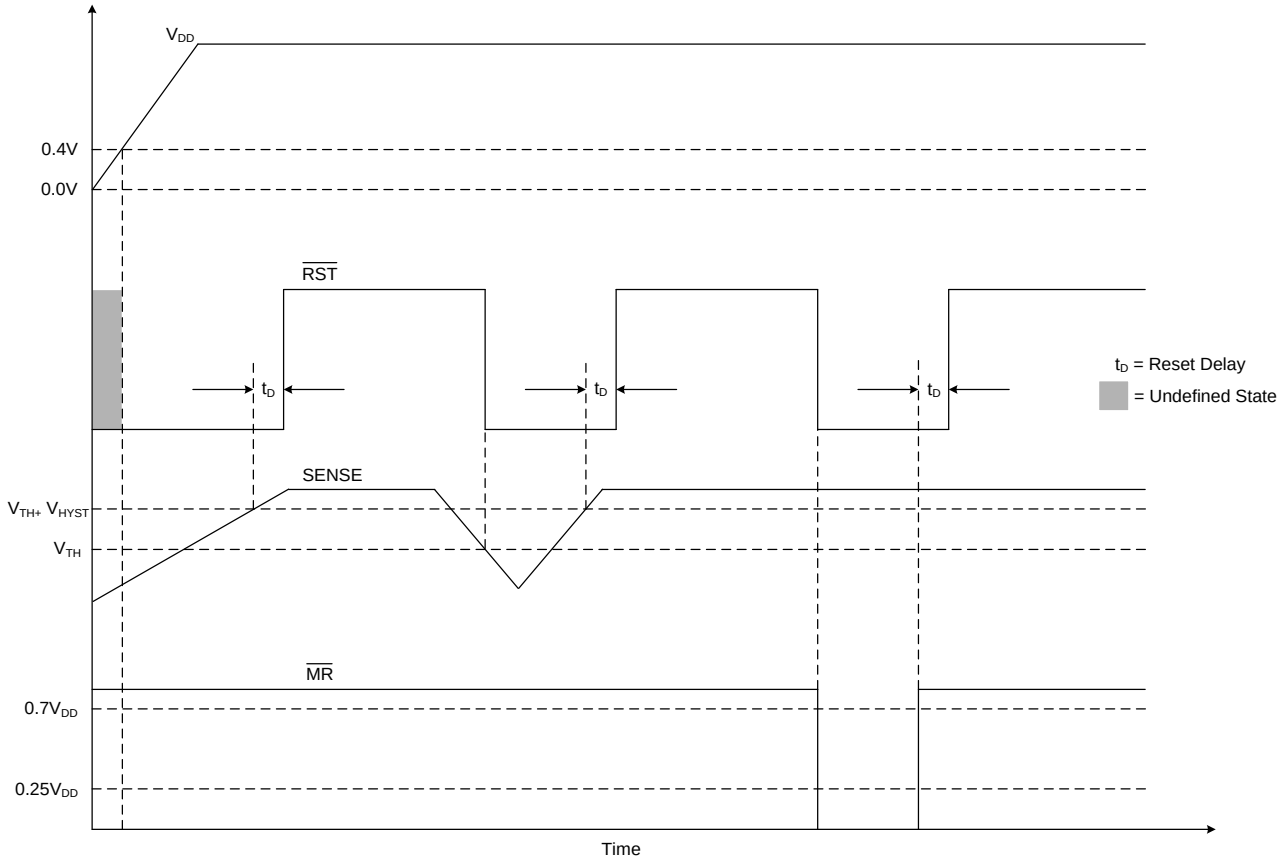


Figure 9. Timing Chart of FP6805AS9/FP6805AD7

Truth Table

$\overline{MR}$	SENSE > V_{TH}	$\overline{RST}$/RST
L	0	L/H
L	1	L/H
H	0	L/H
H	1	H/L

Absolute Maximum Ratings (Note 1)

- Input Voltage Range, V_{DD} ---------- -0.3V to +6.5V
- C_d Voltage Range, V_{Cd} ---------- -0.3V to V_{DD} +0.3V
- Other Voltage Ranges: $V_{\overline{RST}}$, $V_{\overline{MR}}$, V_{SENSE} ---------- -0.3V to +6.5V
- $\overline{RST}$ Pin Current ---------- 5mA
- Power Dissipation @T_A=25ºC (P_D)
  - TSOT-23-3/5/6 ---------- 0.4W
  - TDFN-6 (2mm×2mm) ---------- 0.74W
- Package Thermal Resistance (θ_{JA})
  - TSOT-23-3/5/6 ---------- 250ºC/W
  - TDFN-6 (2mm×2mm) ---------- 136ºC/W
- Package Thermal Resistance (θ_{JC})
  - TSOT-23-3/5/6 ---------- 110ºC/W
  - TDFN-6 (2mm×2mm) ---------- 56ºC/W
- Maximum Junction Temperature (T_J) ---------- +150ºC
- Storage Temperature Range (T_{STG}) ---------- -65ºC to +150ºC
- Lead Temperature (Soldering, 10sec.) ---------- +260ºC

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions

- Supply Voltage, V_{DD} ---------- +1.5V to +6V
- Other Voltage Ranges: $V_{\overline{RST}}$, $V_{\overline{MR}}$, V_{SENSE} ---------- -0.3V to +6V
- Operation Temperature Range (T_{OPR}) ---------- -40ºC to +85ºC
- Operation Junction Temperature Range (T_J) ---------- -40ºC to +125ºC

Electrical Characteristics

(V_{DD}=5V, T_A=25ºC, unless otherwise specified for FP6805S9, FP6805D7)

Parameter	Symbol	Conditions		Min	Typ.	Max	Unit
Input Supply Range	V_{DD}			1.5		6	V
Supply Current (Current Into V_{DD} Pin)	I_{DD}	V_{DD}=5.5V, $\overline{RST}$ not Asserted $\overline{MR}$, $\overline{RST}$, C_d Open			1.5	3	μA
Low-Level Output Voltage	V_{OL}	1.5V≦V_{DD}＜1.8V, I_{OL}=0.4mA				0.3	V
		1.8V≦V_{DD}＜5.5V, I_{OL}=1.0mA				0.4	
Power-up Reset Voltage		V_{OL}(max)=0.2V, $I_{\overline{RST}}$ =15μA, $T_{rise(VDD)}$≧15μs/V				0.4	V
Negative-Going Input Threshold	V_{TH_adj}	Adj. Version		0.396	0.4	0.404	V
Negative-Going Input Threshold Voltage Accuracy	V_{TH}	Adj. Version		-1		+1	%
		Fixed Versions (Note 2)		-1		+1	%
Hysteresis on V_{TH} Pin	V_{HYST}	Adj. Version			1.5	3.5	$\%V_{TH}$
		Fixed Versions (Note 2)			1.5	3.5	
$\overline{MR}$ Internal Pull up Resistance (Note 3)	$R_{\overline{MR}}$			70	110		kΩ
Input Current at SENSE Pin	I_{SENSE}	Adj. Version	$V_{SENSE}=V_{TH}$	-25		25	nA
		Fixed Versions (Note 2)	V_{SENSE}=5.5V		1		μA
$\overline{RST}$ Leakage Current	I_{OH}	$V_{\overline{RST}}$=5.5V, $\overline{RST}$ not Asserted				300	nA
Input Capacitance, Any Pin	C_{IN}	C_d Pin	V_{IN}=0V to V_{DD}		30		pF
		Other Pins	V_{IN}=0V to 5.5V		5		
$\overline{MR}$ Logic Low Input	V_{IL}			0		$0.25V_{DD}$	V
$\overline{MR}$ Logic High Input	V_{IH}			$0.7V_{DD}$		V_{DD}	
Input Pulse width to $\overline{RST}$	t_w	SENSE	$V_{IH}=1.05V_{TH}$, $V_{IL}=0.95V_{TH}$		20		μs
$\overline{RST}$ Delay Time	t_D	C_d=Open	See Timing Chart	156	240	324	ms
		$C_d=V_{DD}$	See Timing Chart			150	μs
		C_d=10nF	See Timing Chart	60	93	125	ms
		C_d=150pF	See Timing Chart	1.07	1.65	2.22	ms
Propagation Delay	t_{pHL}	$\overline{MR}$ to $\overline{RST}$	$V_{IH}=0.7V_{DD}$ $V_{IL}=0.3V_{DD}$		150	4000	ns
High-to-Low Level $\overline{RST}$ Delay		SENSE to $\overline{RST}$	$V_{IH}=1.05V_{TH}$, $V_{IL}=0.95V_{TH}$		20		μs

Electrical Characteristics (Continued)

(V_{DD}=5V, T_A=25ºC, unless otherwise specified for FP6805S8)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input Supply Range	V_{DD}		1.5		6	V
Supply Current (Current Into V_{DD} Pin)	I_{DD}	V_{DD}=5.5V, $\overline{RST}$ not Asserted $\overline{MR}$, $\overline{RST}$, C_d Open		2.5	4	μA
Low-Level Output Voltage	V_{OL}	1.3V≦V_{DD}＜1.8V, I_{OL}=0.4mA			0.3	V
		1.8V≦V_{DD}＜5.5V, I_{OL}=1.0mA			0.4	
Power-up Reset Voltage		V_{OL}(max)=0.2V, $I_{\overline{RST}}$ =15μA, $T_{rise(VDD)}$≧15μs/V			0.4	V
Negative-Going Input Threshold Voltage Accuracy	V_{TH}	Fixed Versions (Note 2)	-1		+1	%
$\overline{MR}$ Internal Pull up Resistance (Note 3)	$R_{\overline{MR}}$		70	110		kΩ
$\overline{RST}$ Leakage Current	I_{OH}	$V_{\overline{RST}}$=5.5V, $\overline{RST}$ not Asserted			300	nA
$\overline{MR}$ Logic Low Input	V_{IL}		0		0.25V_{DD}	V
$\overline{MR}$ Logic High Input	V_{IH}		0.7V_{DD}		V_{DD}	
$\overline{RST}$ Delay Time	t_D		156	240	324	ms
Propagation Delay	t_{pHL}	$\overline{MR}$ to $\overline{RST}$ V_{IH}=0.7V_{DD} V_{IL}=0.3V_{DD}		150	4000	ns
High-to-Low Level $\overline{RST}$ Delay		V_{DD} to $\overline{RST}$ V_{IH}=1.05V_{TH}, V_{IL}=0.95V_{TH}		20		μs

(V_{DD}=5V, T_A=25ºC, unless otherwise specified for FP6805S7)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input Supply Range	V_{DD}		1.5		6	V
Supply Current (Current Into V_{DD} Pin)	I_{DD}	V_{DD}=5.5V, $\overline{RST}$ not Asserted		2.5	4	μA
Low-Level Output Voltage	V_{OL}	1.3V≦V_{DD}＜1.8V, I_{OL}=0.4mA			0.3	V
		1.8V≦V_{DD}＜5.5V, I_{OL}=1.0mA			0.4	
Power-up Reset Voltage		V_{OL}(max)=0.2V, $I_{\overline{RST}}$ =15μA, $T_{rise(VDD)}$≧15μs/V			0.4	V
Negative-Going Input Threshold Voltage Accuracy	V_{TH}	Fixed Versions (Note 2)	-1		+1	%
High-to-Low Level $\overline{RST}$ Delay		V_{DD} to $\overline{RST}$ V_{IH}=1.05V_{TH}, V_{IL}=0.95V_{TH}		20		μs
$\overline{RST}$ Leakage Current	I_{OH}	$V_{\overline{RST}}$=5.5V, $\overline{RST}$ not Asserted			300	nA
$\overline{RST}$ Delay Time	t_D		156	240	324	ms

Note 2: Refer to “Ordering Information”.
Note 3: Not production tested.

Application Information

The FP6805 are supervisory circuits, which monitors critical voltages and asserts reset signal to the subsequent devices. The FP6805 will assert a $\overline{RST}$ (RST) signal when either the SENSE (FP6805S9, FP6805D7) pin voltage drops below V_{TH} or the $\overline{MR}$(FP6805S8, FP6805S9, FP6805D7) pin is driven low. The FP6805 (FP6805S7, FP6805S8, FP6805S9) family can be set to a fixed voltage from 0.8V to 5V, and while the FP6805 (FP6805S9, FP6805D7) can set to any voltage above 0.4V by using an external resistor divider.

Once SENSE (FP6805S9, FP6805D7) pin exceeds the threshold voltage (V_{TH}), an internal timer will keep $\overline{RST}$(RST) low(high) for the reset timeout. After this period, $\overline{RST}$(RST) will go high(low). If SENSE (FP6805S9, FP6805D7) pin falls below the threshold voltage (V_{TH}), $\overline{RST}$(RST) will go low(high) immediately. The user can select any reset delay time from 2ms to 10s by connecting a capacitor between C_d and GND (FP6805S9, FP6805D7).

The FP6805 (FP6805S7, FP6805S8) family $\overline{RST}$(RST) signal is guaranteed to be a logic low (high) for $V_{TH}>V_{DD}>0.8V$. Once V_{DD} (FP6805S7, FP6805S8) pin exceeds the threshold voltage (V_{TH}), an internal timer will keep $\overline{RST}$(RST) low (high) for the reset timeout. After this period, $\overline{RST}$(RST) will go high (low). If V_{DD} (FP6805S7, FP6805S8) pin falls below the threshold voltage (V_{TH}), $\overline{RST}$(RST) will go low (high) immediately.

Whenever V_{DD} (FP6805S7, FP6805S8) pin drops below the threshold voltage (V_{TH}), the internal timer resets to zero and $\overline{RST}$(RST) goes low (high). The internal timer keeps activated only when $V_{DD} > V_{TH}$, and $\overline{RST}$(RST) remains low (high) for the reset timeout interval.

Reset Output

The $\overline{RST}$(RST) output is undefined for voltage below 0.4. If SENSE (FP6805S9, FP6805D7) pin or V_{DD} (FP6805S7, FP6805S8) pin is above its threshold voltage(V_{TH}) and the $\overline{MR}$ (FP6805S8, FP6805S9, FP6805D7) pin is logic high,$\overline{RST}$(RST) will be driven to a logic high(low). If either SENSE (FP6805S9, FP6805D7) pin or V_{DD} (FP6805S7, FP6805S8) pin falls below V_{TH} or $\overline{MR}$ (FP6805S8, FP6805S9, FP6805D7) pin is driven low,$\overline{RST}$(RST) will be asserted. On $\overline{MR}$(FP6805S8, FP6805S9, FP6805D7) pin is logic high again and SENSE (FP6805S9, FP6805D7) pin or V_{DD} (FP6805S7, FP6805S8) pin is above V_{TH}, $\overline{RST}$(RST) will hold logic low(high) for a specific reset delay time. Once the reset delay time expires, $\overline{RST}$(RST) will drive logic high(low). Since the reset output of FP6805 is open drain, connecting a pull-up resistor between $\overline{RST}$ (RST) and V_{DD}, allows either device to assert reset (Figure 10), the pull up resistor should be larger than 10kΩ.

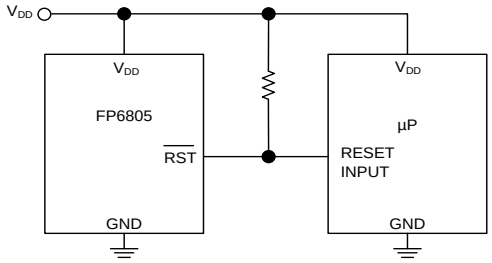


Figure 10. Interfacing to µPs with Bidirectional Reset I/O

SENSE Input

Use SENSE to monitor system voltage. If SENSE (FP6805S9, FP6805D7) pin drops below V_{TH}, the $\overline{RST}$(RST) will be asserted. A 1nF to 10nF bypass capacitor can be put between SENSE and GND to reduce additional noise immunity of SENSE pin. The FP6805 (FP6805S9, FP6805D7) can be set to any voltage above 0.4V.

$$V_{TH}=(1+\frac{R1}{R2})\times 0.4$$

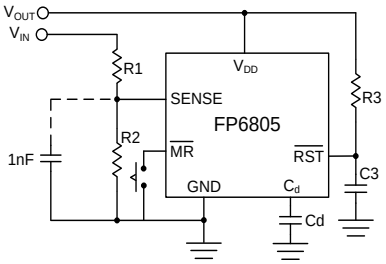


Figure 11. Monitor a User-Defined Threshold Voltage

Thermal Consideration

The power handling capability of the device will be limited by maximum 150°C operation junction temperature. The power dissipated by the device will be estimated by $P_D=(T_{J(MAX)}-T_A)/\theta_{JA}$. The power dissipation should be lower than the maximum power dissipation listed in “Absolute Maximum Ratings” section.

Application Information (Continued)

Manual Reset Input

Many μP-based products require manual reset capability, allowing the operator or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ (FP6805S8, FP6805S9, FP6805D7) pin asserts reset. When $\overline{MR}$ returns high and SENSE (FP6805S9, FP6805D7) is above threshold voltage for the reset delay time, $\overline{RST}$(RST) will de-asserted. This input has an internal 110kΩ pull-up resistor, so it can be left open if it is not used. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1μF capacitor from $\overline{MR}$ to ground provides additional noise immunity. Figure 12 shows how $\overline{MR}$ can be used to monitor multiple system voltages. If the $\overline{MR}$ signal does not reach VDD, there will be additional current draw from V_{DD} through $\overline{MR}$ by internal pull-up resistor. To minimize current draw, a logic-level FET can be used as illustrated in Figure 13.

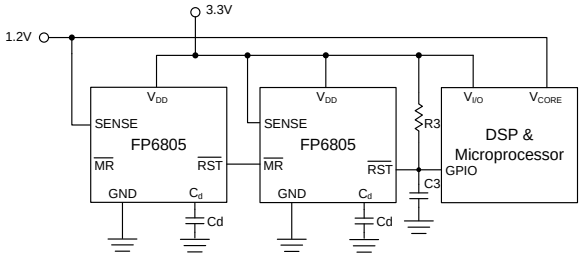


Figure 12. Applying $\overline{MR}$ to Monitor Multiple System Voltage

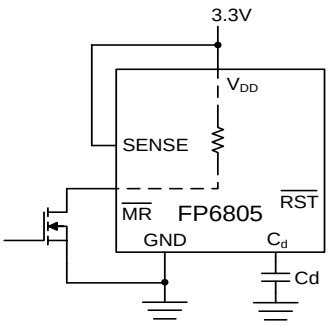


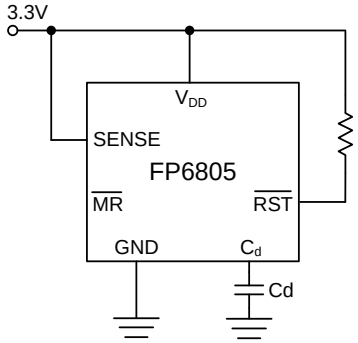
Figure 13. Applying an External NMOSFET to Minimize I_{DD} When $\overline{MR}$ Signal does not reach V_{DD}

Choose the Reset Delay Time

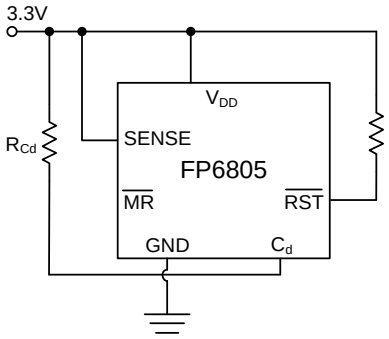
Figure 14(a). shows that the FP6805 (FP6805S9, FP6805D7) sets the $\overline{RST}$ (RST) delay time by connecting a capacitor between C_d and GND. And user can define program time between 2ms and 10s.

The capacitor C_d must be larger than 150pF. A given delay time of the capacitor value can be calculated by using the following equation:

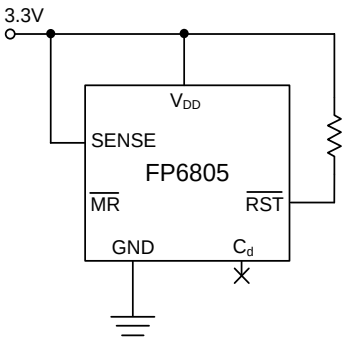
$$Cd(nF)=\left[t_D(s)-0.28\times10^{-3}(s)\right]\times\frac{75}{0.7}$$



(a)Capacitor adjustable delay time



(b)C_d Pin Connected to V_{DD} through a resistor



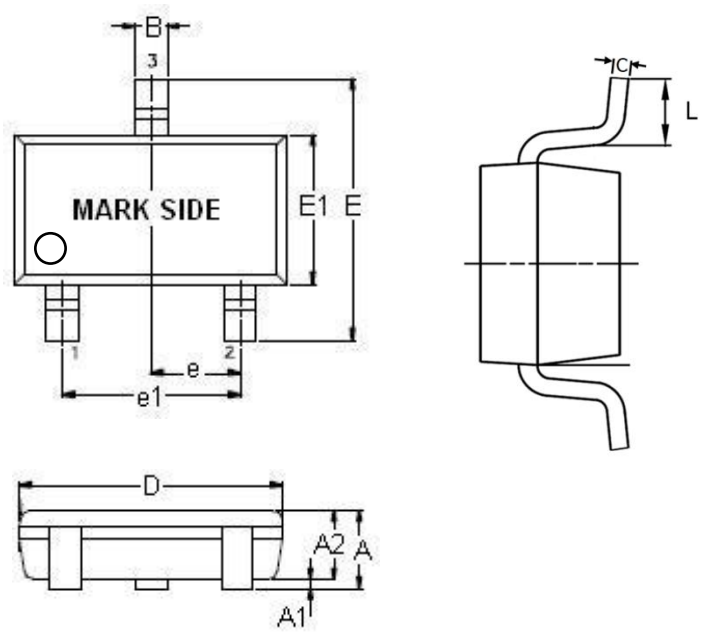
(c)C_d Pin Open

Figure 14. Applying to Set the $\overline{RST}$(RST)Delay Time

Figure 14(b). shows that the FP6805 (FP6805S9, FP6805D7) sets the $\overline{RST}$ (RST)delay time by connecting a resistor with 50kΩ to 300kΩ between C_d and V_{DD}. And user can set delay time 0ms.And user can program delay time 240ms by open C_d Pin. The circuit can refer figure 14(c).

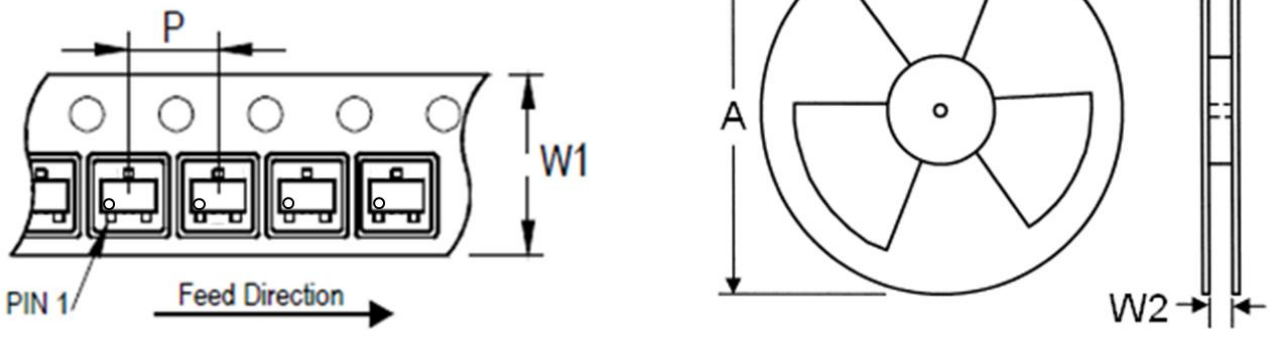
Outline Information

TSOT-23-3 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.90
A1	0.00	0.10
A2	0.70	0.80
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
C	0.08	0.20
L	0.30	0.60

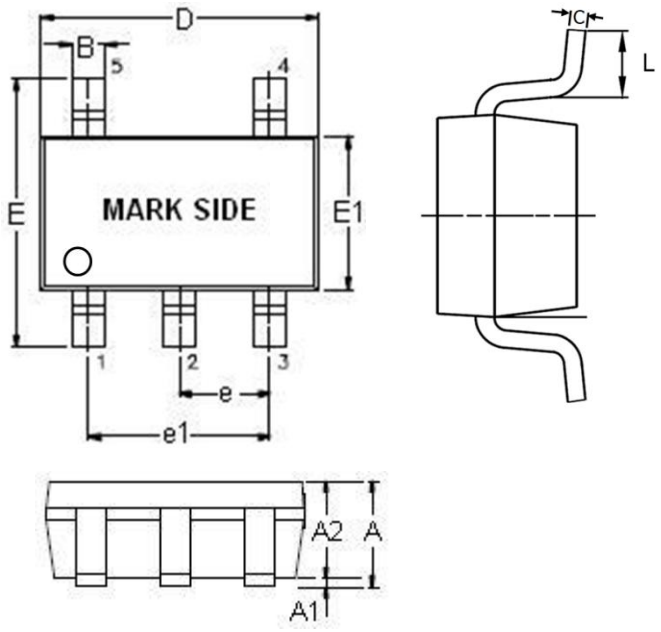
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

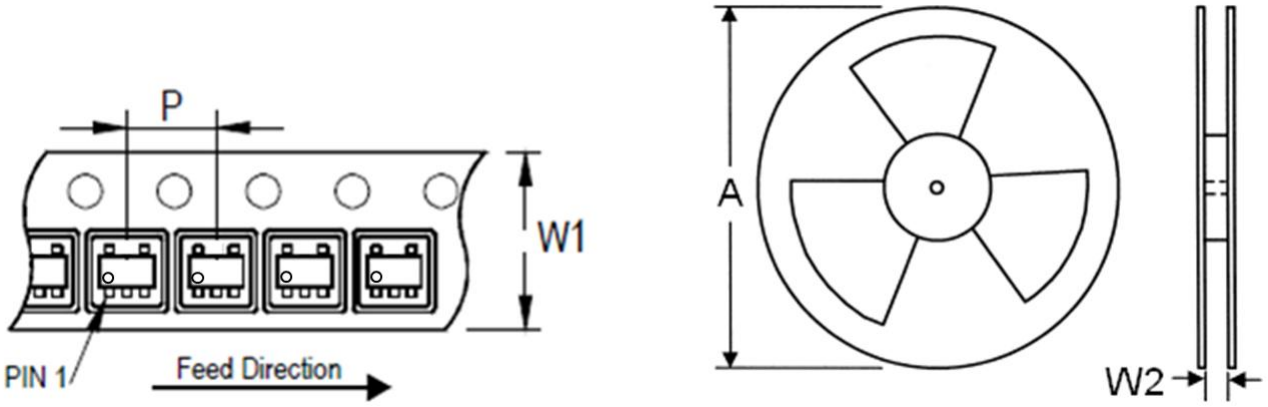
Outline Information (Continued)

TSOT-23-5 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.90
A1	0.00	0.10
A2	0.70	0.80
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
C	0.08	0.20
L	0.30	0.60

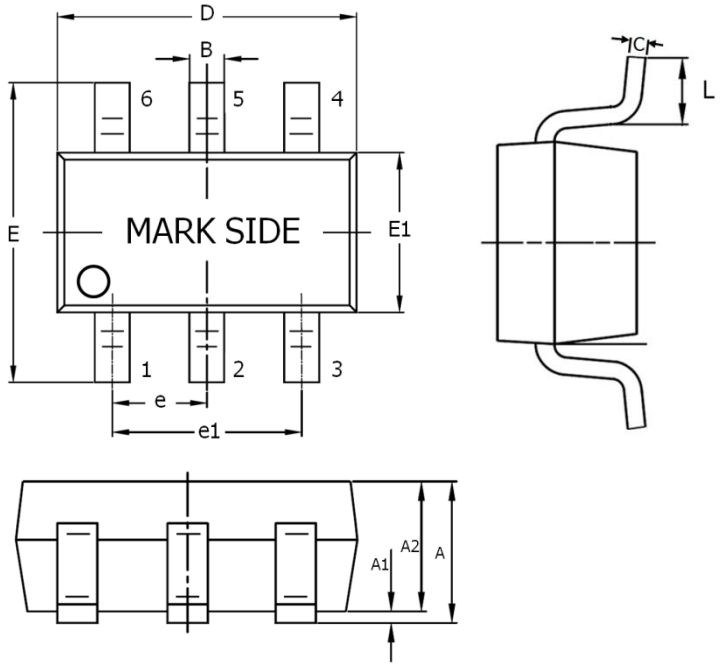
Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

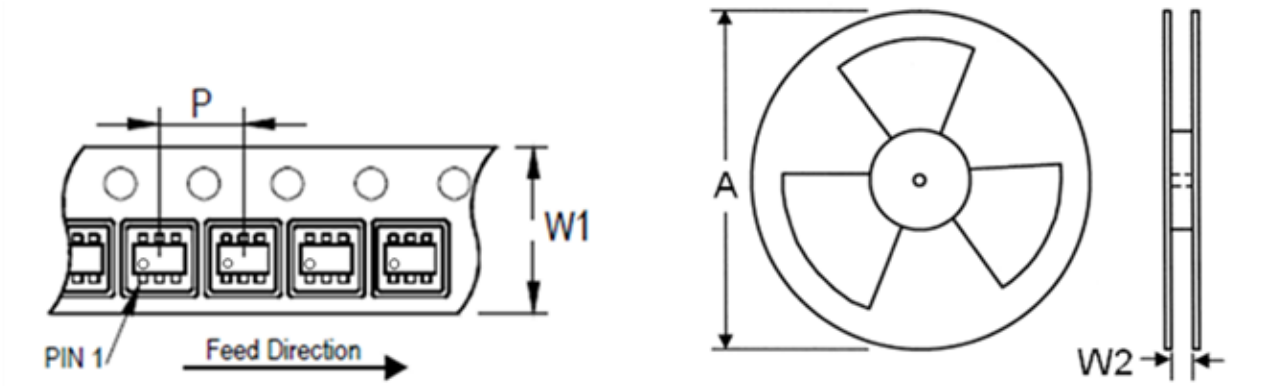
Outline Information (Continued)

TSOT-23-6 Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.95
A1	0.00	0.10
A2	0.70	0.85
B	0.30	0.50
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.70
e	0.90	1.00
e1	1.80	2.00
C	0.08	0.20
L	0.30	0.60

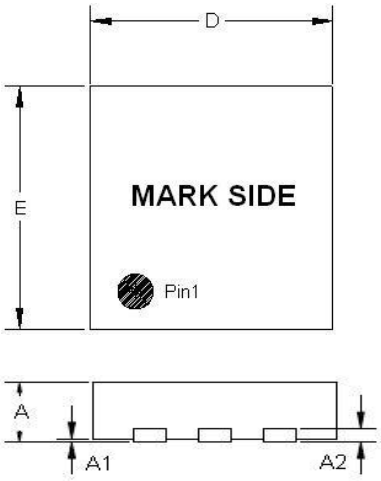
Carrier Dimensions

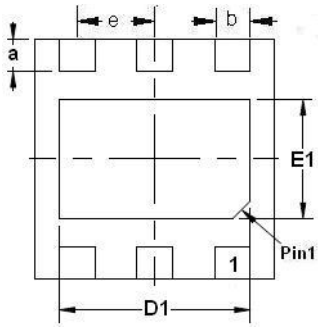


Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	300~1000	3,000

Outline Information (Continued)

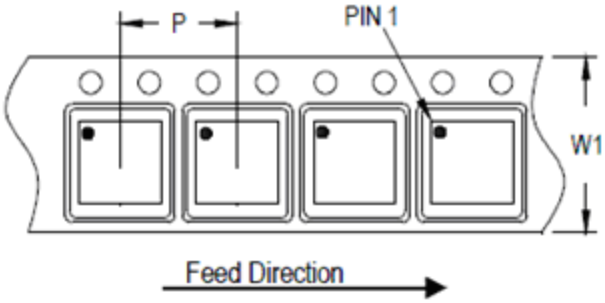
TDFN-6 (2mm×2mm) (pitch 0.65mm) Package (Unit: mm)

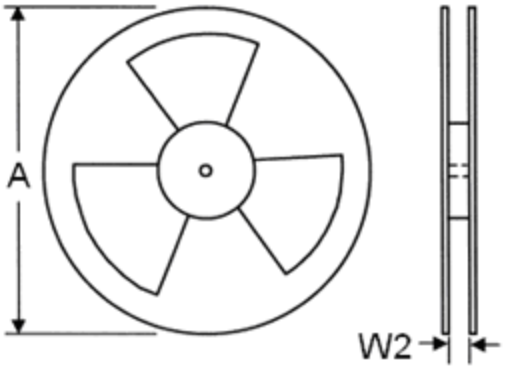




SYMBOLS UNIT	DIMENSION IN MILLIMETER	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A2	0.18	0.25
D	1.90	2.10
E	1.90	2.10
a	0.20	0.40
b	0.20	0.40
e	0.65 BSC	
D1	1.00	1.50
E1	0.50	0.86

Carrier Dimensions





Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
8	4	7	180	8.4	400~1000	3,000